Encapsulation of Large, Densely Populated Die with Small Gap

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Abstract

The introduction of underfill, a real breakthrough in the flip chip package industry, gave the solder interconnection technology an unforeseen mechanical robustness and a significant increase in flip-chip solder fatigue resistance. Derivatives from this technology (i.e., plastic ball grid arrays-PBGA, ceramic ball grid array-CBGA, chip scale packages-CSP, etc.) have been developed in recent years. In essence, these new technologies are meant to mimic the product robustness and reliability performance of the original controlled collapse chip connection (C4) first used by IBM on solid logic technology (SLT) for flip chips in the early sixties. These new technologies were developed to increase both mechanical robustness and fatigue resistance. New interconnection geometry, using essentially the same solder materials as the original C4 joints, were introduced to overcome larger mismatches in components displacements during temperature excursions and to support larger loading such as heatsinks, etc. For electronic packaging, the use of these new interconnections has been as successful as the original C4 technology. However, the environments for these packages became increasingly demanding. Failure mechanisms, believed to be eliminated, or at least alleviated by the new package designs, are again threatening their integrity and reliability. Dynamic loading, which is induced during vibration and mechanical shocks, results in reliability detractors for CSP and DCA packages in particular. Analytical models and simulation of these mechanisms are proposed. Reliability requirements for flip chip (FC), in particular large die and flip chip on board (FCOB) also referred as direct chip attach (DCA), mandate underfill or encapsulation processes. These processes are well characterized and commonly used on manufacturing lines across the industry to meet the performance and quality goals for electronic packages. New package geometries (smaller gaps, denser arrays, and longer flow distances) that are being developed pose new challenges to the underfilling process as practiced today. For example, new constraints on fluid flow paths will likely require materials with altered chemistries and smaller particle sizes. In addition, the flow out time with traditional materials in these new applications could cause productivity issues on production lines. This paper describes key parameters affecting the flow-out time with new fluid formulations on large test die with small PCB-to-chip gaps.

Keywords: flip chip, underfill, packaging, capillary flow, reliability

Introduction

The added functionality and reduced size requirements for electronic devices is driving new technical requirements for packaging flip chip devices. This added functionality is in turn creating denser interconnect requirements and hence reduced ball size and pitch distances. Levels of strain tolerable in the package are directly related to the size of the package and the environment during regular field operation. The field environment has become very convoluted for today's electronic package components. Consumer product environments are rather complex. The temperature excursions (the number of on-off power cycles, etc.), can at best be defined in terms of probabilities that may often be truncated, and can seldom be accurately defined deterministically. New handling requirements for consumer products are challenges that package designers need to address early in the product development cycle. Traditionally, the fatigue detractor was the primary reliability concern for flip chip-type technology (i.e., DCA and CSP) [1]. Today, mechanical handling and dynamic loading applied to packages during fabrication and/or field environment operation are the biggest reliability issues. These reliability issues are most apparent in applications where CSPs are used in portable electronics such as, cellular phones, pagers, digital cameras, and a growing list of smaller, more functional electronic devices. The geometry of the CSP, compared to that of the traditional DCA interconnection, offers many reliability advantages. Many new package designs have dispense gaps approaching 25 μm. In addition, added semiconductor functionality requirements are driving increases in the length and width of die. In some cases die are exceeding 25 mm x 25 mm. These changes to chip geometry have posed challenges to the traditional underfill process. Several of these challenges include complete gap fill, void formation and fluid underfill time. Achieving the complete fill of the die-to-substrate gap is an increasingly difficult task. Densely populated die create challenging flow paths for capillary action to overcome. Add the shrinking gap and larger flow distances, and completing the fill will push capillary underfill to its limit. At some point, the die size, gap, and bump population will create a geometry that will require either new materials or new processing to achieve a complete fill. An additional challenge revolves around void formation. Larger dispense areas with localized dense ball populations are anticipated to be more difficult to underfill void free. Thermal gradients from non-uniform substrate heating or irregularities from non-uniform solder bump distribution may lead to an uneven flow front. This uneven flow increases the chances of entrapping air during flow out [2]. Reduced gaps and longer flow distances lead to longer underfill processing time. This has a negative impact on underfilling production line throughput. Experimental results identified in this paper demonstrate that newer underfill fluids and processes extend the traditional capillary underfill process. These new materials are capable of underfilling geometry that is at the limit of current board fabrication technology.

Process Trends

Several processes are available to underfill electronic components. These include capillary underfill and proposed techniques such as transfer molding, pressure assisted underfill, and no-flow underfill. Capillary underfill remains as the industry standard method for underfilling flip chip packages. Traditional underfill dispenses fluid at one or more sides of a die attached to a substrate. Capillary forces draw the fluid underneath the die. In some applications, an additional dispense pass is made around the die perimeter to form a fillet. This fillet enhances the low cycle fatigue endurance of the interconnections.

Transfer molding is another technology that is being investigated for underfilling die. This process requires a mold or cavity to completely encompass the device. A small entrance on one end allows the fluid to enter the underfill cavity and an exit orifice at the other end allows the air underneath the die to escape. The fluid is pressurized, 180 MPa, creating a pressure differential between the entrance side and exit side of the die increasing the speed of the underfill, and forcing the fluid flow underneath the die.

While transfer molding is widely used for encapsulating semiconductor components, there are serious drawbacks when underfilling large die with small gaps. These include availability of appropriate fluid formulations, void formation, high pressure, in the excess of 200 MPa potentially can damage the fragile interconnection and the shrinkage resulting from this high pressure, about 30% greater than compression molding yielding high strains [3]. Complex tooling and maintenance is another detractor for this technology In order for transfer molding to work with today's flip chips, the current molding materials must be reformulated to accommodate smaller filler size and lower curing temperatures as well as having low alpha particle emission. Another concern is that fast fluid flow, although the Reynolds number is of the order unity, has a tendency to form voids in the presence of obstacles, such as interconnections. Add to this, high fluid pressures can introduce significant tensile forces normal to the die and substrate. These forces may crack the die and/or solder bumps (cracking interconnections). And also, the requirement of a complete molding cavity adds tooling complexity. This is especially true with advanced package requirements, e.g., lids and heat sinks, requiring the tooling to leave the die backside completely free of mold material.

The compression flow process, commonly referred to as "no-flow underfill", involves dispensing an underfill material prior to die attach. The die is then placed onto the substrate, compressing the pre-dispensed adhesive. The compression force required to properly seat the die is a function of the fluid volume, fluid properties, die area, ball density, gap size, and compression rate. A cure/reflow step completes the process. New fluid materials with improved CTE properties (for lower filler percentages) need to be developed in order to make the no-flow process viable for packages with large solder bump populations (large die). In addition, the underfill material is seen as an inhibitor to the self-alignment properties of the traditional reflow process. Finally, it is anticipated that higher bump densities will increase the presence of voids (shadow voids) and the higher die placement force may damage the die [4].

Material Trends

Fluid material manufacturers are continuously improving underfill fluid properties. Several new underfill fluids on the market address the requirements for densely populated large die with small gaps. These requirements include low viscosity, small filler sizes and other desired physical properties. Fluid formulators have improved underfill fluid characteristics by lowering viscosity, elastic modulii, contact angle, and filler particle size while maintaining low CTE's (25 to 35 ppm/°C). The main advantages of lower viscosity fluid are that they tend to flow faster and they are less sensitive to void formation. Reduced elastic modulii minimizes the propensity to die cracking, in particular, when subjected to low temperatures after reflow. Smaller filler particle sizes are essential when flowing through the narrow passages associated with denser ball grids and small die gaps. In addition, smaller particles are less affected by the sieve action of dense interconnect patterns avoiding the issue of filler separation and keeping filler distribution uniform. CTE matching between the interconnections and cured fluid results in best cycle fatigue endurance.

Experiments

Several experiments were run to analyze the underfill process. The experiments benchmarked the flow behavior of new and traditional underfill fluids using capillary underfill techniques.

Two test vehicles (T/V) were utilized to characterize the underfill process. One T/V consisted of a small die with a large gap (SDLG), See Figure 1. This form factor was used to compare flow of various fluid formulations including traditional underfills and new formulations. The SDLG test vehicle was built on a 1.5-mm thick FR-4 substrate. Three pads with a mean of 150 μm height were etched in the copper foil to support the glass "die" near the edges. A piece of clear glass 11.0 mm x 11.0 mm square and 0.7 mm thick was secured at opposite corners with two drops of UV adhesive.

Figure 1-Small Die Large Gap Test Vehicle

The second T/V consisted of a larger die with small gap (LDSG) and about 22,500 bumps in a fully populated array. See figure 2. This form factor was used to simulate the effect of those changes on fluid flow. The LDSG test vehicle was also built on a 1.5 mm thick FR-4 substrate. A uniform footprint (bump pattern) was obtained by etching the copper foil. A tin plating was applied to the resultant bump pattern. The size of a bump was 75 µm in diameter and 45 µm high. The bump pattern consisted of a uniform array of 22,500 bumps on 150 µm pitch. A piece of clear glass 25 mm x 25 mm square and 0.7 mm thick was attached with two drops (∅ 0.75 mm) of surface mount adhesive.

Figure 2-Bumped Test Package (LDSG)

Traditional Underfill

The capillary action flow between two parallel plates can be derived on plausible grounds using laminar flow theory and thermodynamic principles of fluid surface curvature dependence on pressure differential across the surface as stated by the Young-Mills equation,

$$P_i - P_j \equiv \Delta P_{ij} \propto \tfrac{1}{r_x} - \tfrac{1}{r_y}$$

Where ***r*$_k$** is the radius of curvature along the ***k*** axis. Applying the conservation of momentum during the underfill flow and combining with the above equation, one would arrive at the popular expression for capillary underfill flowout time, t(x), can be written as

$$t\left(\chi\right)\Big|_{\chi=L} = \frac{3\mu\cdot L^2}{\Gamma\cdot h\cdot\cos\theta}$$

where µ is the coefficient of viscosity, L is the flow length, Γ is the fluid surface tension, h is the gap height, θis the contact angle. Both test vehicles were used to evaluate the underfill materials under capillary conditions. The tests were performed using Asymtek automated underfill dispensing equipment. For these tests the substrates were allowed to come up to temperature and then a line of fluid was applied to one side of the test die. For the SDLG packages 55 mg of fluid was applied. For the LDSG package 90 mg of fluid was applied. Time was measured between the start of dispense and the completion of underfill with a stop watch. The experiments were run on a range of temperatures and four candidate fluids. The candidate fluids included new and traditional fluid formulations. Figure 3 below depicts experimental results of capillary underfill flowout times for LDSG and SDLG for two different materials. The solid lines represent the normalized data to that of the LDSG and the one filled material. From this graph one can assert that the equation for capillary flow times is quite adequate even for such large die with small gaps.

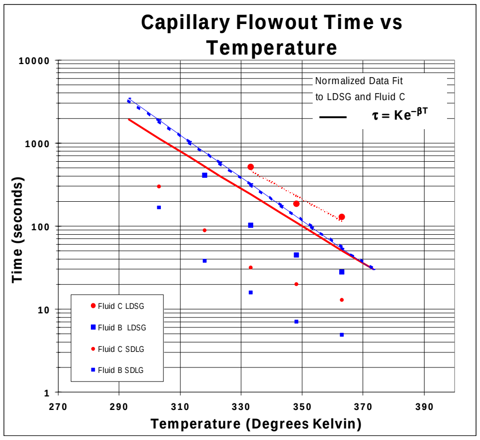

Figure 3- Unassisted Capillary Underfill

Fluid	Visc @ 25C	Tg, C	CTE	Filler ∅
A	2300 cps	140	45 ppm/C	5 µm
B	4500 cps	135	50 ppm/C	No filler
C	10000 cps	110	31 ppm/C	1.5 µm
D	4700 cps	133	25 ppm/C	<27 µm

Table 1- Test Fluid Properties

After completing the experiments several observations were made:

- All of the fluids tested were able to successfully underfill the SDLG test substrate.
- Only two of the fluids tested were able to successfully underfill the LDSG test substrate.
- The substrate/die temperature significantly affected the speed of the underfill. See Figure 3.
- The LDSG test package took longer to underfill than the SDLG test package.

Conclusions

This C4 technology, in general, needs to be properly encapsulated when the die is placed on FR4-type carriers where CTE mismatches are significant.

As packages get larger, fatigue life is likely to become more of a detractor; even CSP packages may become vulnerable to low-cycle fatigue-like problems.

Traditional capillary underfilling can be extended to large, densely populated die with small gaps using newer fluids already available. New fluid formulations are needed to continue to improve the unassisted capillary underfill time when used with these larger, more densely populated dies. Tests have shown that the reliability of a package increases with a lower encapsulant CTE [5].

As the trend for larger die and smaller gaps continue, challenges to packaging processes will continue to rise. Material and processing developments, will allow the underfill process to successfully meet these challenges, making underfill the standard packaging process for all flip chip applications.

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References

[1] H.Quinones, K.Puttlitz, “Flip Chip Solder Interconnections: A Reliability Perspective,” Packaging Conference, Orlando Fl, 1996.

[2] Chien-YiHuang, “DCA Encapsulation Process Study,” State University of NY at Binghamton, March 1996.

[3] Rao R. Tummala, E. J. Rymaszewski, “Microelectronics Packaging Handbook,”Van Nostrand Reinhold 1989, Chapter 8.

[4] Pascarella, N. and Baldwin, D., Compression Flow Modeling of Underfill for Low Cost Flip Chip Assembly, Electronic Components and Technology Conference, Seattle, WA, May 1998

[5] Giesler, J., O'Malley, G., Williams, M., and Machuga, S.C., “Flip Chip on Board Connection Technology: Process Characterization and Reliability”, *IEEE Comp., Packag., Manufact. Technol.*, vol. 17, pp. 256-263, 1994.